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ENCLOSURES (*Check all that apply*)

- [x] Fee Transmittal Form
  - [x] Fee Attached
- [ ] Amendment/Reply
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Signature	Ellsworth R. Roston
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Donna M. Colon

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of	Examiner: Zervigon, R.
Inventor: Laptev, P.	Group Art Unit: 1763
Serial No. 09/829,587	Confirmation No.: 7932
Filed: 04/09/2001	Client ID/Matter No.: SPUTT-56141
For: SYSTEM FOR, AND METHOD OF, ETCHING A SURFACE ON A WAFER	Date: November 5, 2003
	Los Angeles, California 90045

APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

1. Real Property Interest

   Sputtered Films, Inc., the assignee of record of the application.

2. Related Appeal and Interferences

   None

3. Status of Claims

Claims 1-21 and 43-51 have been rejected by the Examiner on the basis of prior art cited by the Examiner. These are the only claims in the application.

4. Status of Amendment

On October 30, 2003, applicant filed an amendment under Rule 116 to make minor changes in claims 1, 3, 8, 9, 48 and 49, such minor changes having been noted by applicant's attorney in studying the claims to prepare this appeal brief. The changes in the claims do not affect the scope of the claims. They are being made to make the claims consistent with applicant's specification and drawings as originally filed. The Examiner has not had an opportunity to act upon these proposed changes. Applicant believes that the Examiner will agree to enter the amendment because the amendment corrects informalities noted by applicant's attorney in the claims without affecting the scope of the claims.

5. Summary of the Invention

Copy page 7, line 3, to page 15, line 13 of the specification.

6. Issues

a. Is applicant the first to provide a smooth and uniform deposition on the surface of a layer in a wafer?

b. Is applicant the first to provide two (2) electrical fields, one (1) to produce an ionization of molecules of an inert gas and the other to etch the surface of a layer in the wafer with a low energy from the ionized molecules to produce a smooth and uniform surface on the wafer?

c. Is applicant the first to provide two (2) electrical fields, one with a high strength to ionize molecules of an inert gas and the other with a low strength to etch the surface of the layer with the ionized gas and provide the surface with smooth and uniform characteristics?

d. Is applicant the first to provide two (2) electrodes, the first spaced further from the wafer than the second and the second contiguous to, but spaced from, the wafer and to use the first electrode in providing an electrical field with a high strength and to use the second electrode in providing an electrical field with a low strength?

e. Is applicant the first to provide a first electrode and a first electrical conducting member disposed relative to each other for producing a first electrical field of a high strength to ionize molecules of an inert gas and for providing a second electrode and a second electrical conducting member disposed relative to each other for producing a second electrical field of a low strength to the surface of the layer in the wafer to provide the surface of the wafer with smooth and uniform characteristics?

f. Is applicant the first to dispose the second electrode in contiguous, but spaced, relationship to the wafer to obtain the production of two capacitors in series, one having a low impedance and the second having a high impedance whereby the high impedance limits the flow of current through the capacitor and provides for the production of a smooth and uniform surface on an insulating layer in the wafer?

g. Is applicant the first to provide a dielectric of the molecules and ions of the inert gas as an insulation layer and to provide the insulation layer as the dielectric in the second capacitor?

h. Is applicant the first to define the plates of the capacitor of high impedance by the first electrode and by the electrically conductive layers in the wafer and to define the plates of the capacitor of low impedance by the electrically conductive layers in the wafer and the charge provided by the ions of the inert gas?

i. Is applicant the first to provide a wafer having a floating potential relative to the negative potentials on the first and second electrodes and relative to a reference potential in an apparatus for etching a surface of an insulating layer in a wafer to provide the surface with smooth and uniform characteristics?

7. Grouping of Claims

The Examiner has grouped applicant's claims into two (2) groups as follows:

a. Claims 1-4, 7-9, 11, 14-16, 19-21, 43-47 and 51. These claims have been rejected under 35 U.S.C. 102(b) as being anticipated by Koshimizu patent 5,980,687 and demonstrated by Mountsier patent 5,810,933.

b. Claims 5, 6, 10, 12, 13, 17, 18, 20, 48, 49 and 51. These claims have been rejected under 35 U.S.C. 103(a) as being unpatentable over Koshimizu patent 5,990,687 in view of Mountsier patent 5,810,933.

Applicant respectfully disagrees with the grouping of claims by the Examiner. Applicant proposes the following grouping of the claims and indicates below, for each group, how the claims in that group are patentably distinguished from the claims in the other groups.

i. Claims 1 and 4. These claims recite a combination that includes first and second electrodes wherein the first electrode is constructed, disposed

and biased to ionize molecules of an inert gas and the second electrode is constructed, disposed and biased to obtain a movement of ions of the inert gas to a wafer at a low and controlled speed for an etching of the insulating layer of the wafer by the ions at the low and controlled speed.

ii. Claims 2, 5, 6, 9, 16, 45, 46, 47 and 50. In addition to reciting the first and second electrodes, these claims recite first and second electrical conducting members respectively associated with the first and second electrodes to create first and second electrical fields.

iii. Claim 3. First and second sources of alternating voltages are provided for creating biases respectively on the first and second electrodes, the biases on the electrodes being negative direct voltages and the bias on the second electrode being less than the bias on the first electrode.

iv. Claims 7, 21, 43 and 44. First and second sources of alternating voltage respectively produce voltages of high and low magnitudes on, or in the vicinity of, the first and second electrodes for the creation respectively of first and second electrical fields of high and low strength in an enclosure. The wafer is disposed relative to the ions of an inert gas to receive an etching of a low magnitude on the surface of the insulating layer in the wafer.

v. Claim 8. The second electrode is contiguous to, but spaced from, the wafer.

vi. Claims 11, 14, 19, 48, 49 and 51. The wafer is disposed relative to the second electrode to create the first and second capacitors, one having a low impedance and the other having a high impedance.

vii. Claims 10, 12, 17, 18 and 20. The wafer is disposed between the first and second electrodes and a floating potential is provided on the wafer relative to the negative potential on the first and second electrodes.

viii. Claim 13. The wafer is disposed in a spaced, but contiguous, relationship to the second electrode to create a first capacitor between the second electrode and the wafer and to create a second capacitor between the wafer and the ions of the inert gas in the enclosure.

ix. Claim 15. The first capacitor includes a dielectric of the molecules and ions of the inert gas and the second capacitor includes a dielectric constituting the insulating layer(s) in the wafer.

8. Argument.

a. General Discussion Relating to the Differences Between Applicant's Invention (Not Applied Specifically to any of the Claims) and the prior art. Claim 1-4, 7-9, 11, 14-16, 19-21, 43-47 and 50 have been rejected under 35 U.S.C. 102(b) as being anticipated by Koshimizu patent 5,980,687 and demonstrated by Mountsier patent 5,810,933. The Examiner has had to cite two (2) references in combination to reject these claims. The claims are accordingly not anticipated by Koshimizu.

The Examiner has applied the electrodes 116 and 110, the wafer W attached to the electrode 116 and the conduit 202 in Koshimizu against claims 1-4, 7-9, 11, 14-16, 19-

21, 43-47 and 50. The citation of the electrodes 116 and 110 against these claims constitutes an aggregation. This results from the fact that the electrode 110 has no effect on the production of a deposition on the wafer W attached to the electrode 116. Similarly, the electrode 116 has no effect on the production of a deposition on the wafer W attached to the electrode 110. This may be seen from the following statement in Koshimizu at column 6, lines 27-30:

> "Moreover, in the etching apparatus 100, wafers W fixed on the first and second susceptors 110 and 116 can simultaneously be subjected to the same etching process, thereby increasing the throughput of the apparatus."

A simultaneous deposition of two (2) wafers, each deposition performed independently of the other, does not mean that the apparatus for producing the two (2) wafers constitutes a combination.

Stating the results simply, the operation of the electrode 110 in Koshimizu does not affect the deposition produced on the upper one of the wafers as in Figure 3 by the voltage on the electrode 116. Furthermore, as will be discussed in detail subsequently, Mountsier does not teach or demonstrate what Koshimizu allegedly discloses but does not make operative.

The Examiner has admitted on page 8 of the Office Action dated October 11, 2003 that Koshimizu discloses an aggregation rather than a combination. This may be seen from the following statement by the Examiner at the top of page 8 of the Office Action:

> "The Examiner agrees that Koshimizu operates the second 110 and first electrodes 116 independently of each other to process any number of wafers including one." (Underlining supplied).

The word "independently" indicates that Koshimizu's apparatus is an aggregation.

Since the Koshimizu apparatus constitutes an aggregation, Koshimizu discloses two substantially identical combinations. One combination involves the electrodes 116 (but not the electrode 110) and the wafer W closest to the electrode 116 and the other involves the electrode 110 (but not the electrode 116) and the wafer W closest to the electrode 110. As a result, Koshimizu does not disclose a combination involving two (2) electrodes. There may be two (2) separate combinations in Koshimizu, but the two (2) combinations constitute an aggregation. There is accordingly only a simple electrode (116 or 110) in each of the two (2) separate combinations in Koshimizu.

All of applicant's claims involve a combination of two (2) electrodes. These two (2) electrodes are interrelated in a single combination. Because of this, there is a fundamental difference between the single combination recited in applicant's claims and the two (2) independent combinations in Koshimizu.

There is another fundamental difference between the single combination recited in applicant's claims and the two (2) independent combinations constituting an aggregation in Koshimizu. One of applicant's electrodes (24) is involved in producing argon ions from argon molecules. The electrode 24 receives a high voltage. The other (22) of

applicant's electrodes is involved in etching a surface 12 of an insulated layer 14 in a wafer 16 at a low and controlled voltage and at a low energy to provide a smooth surface on the layer. In contrast, the electrodes 116 and 110 in Koshimizu perform the same function. Neither of the electrodes 116 and 110 in Koshimizu etches a surface of the wafer W at a low and controlled rate to provide the etching with a smooth surface.

There is a further significant difference between applicant's invention and Koshimizu. As shown in Figure 4a and 4B of applicant's drawings, applicant provides two (2) capacitors 52 and 54 in a series relationship. One of these capacitors has a high impedance. This limits to a low value the current flowing through the capacitors. This low current causes the etching of the material on the surface 12 of the layer 14 to be smooth and uniform.

In the Office Action dated July 11, 2003, the Examiner has made a number of statements about the construction and operation of the Koshimizu apparatus that are not supported by the specification and drawings in Koshimizu. These include the following:

i. According to the Examiner on page 4 of the Office Action, a first member 104 is disposed adjacent the first electrode 116 for providing a reference potential different in magnitude from the bias on the first electrode. However, Koshimizu does not disclose the magnitude of the voltage on either of the electrodes 116 and 110. Thus, the Examiner's statement about voltage is unsupported. Furthermore, Koshimizu does not disclose the distance between the electrode 116 and the container 104. However, judging from Figure 1 in Koshimizu, the electrode 116 and the container

104 do not appear to be adjacent each other. Koshimizu also does not disclose that the electrode 116 and the container 104 produce a first electrical field.

ii. Koshimizu states on page 4 of the Office Action that the annular rail 204 is adjacent the electrode 110 for providing the reference potential to create a second electrical field. The voltage applied to the electrode 110 is not disclosed in Koshimizu. Koshimizu does not disclose the application of any voltage to the electrode 110 or the annular rail 204. Koshimizu does not disclose that the annular rail 204 is adjacent to the electrode 110. Figure 3 in Koshimizu does not indicate any such adjacent relationship. It would appear that no electrical field is created by the electrode 110 and the annular rail 204. This is particularly true since the annular rail 204 appears to be floating because it is disposed on the insulating support plate 108.

iii. There is a statement by the Examiner on page 4 of the Office Action that a first source 134 of alternating voltage creates a bias on the electrode 116, this bias being a negative direct voltage. There is no indication in Koshimizu that the alternating voltage from the source 134 creates a bias or a negative direct voltage. The Examiner attempts to use applicant's disclosure to support his statement that there is a bias of a negative direct voltage on the electrode 116. However, Koshimizu does not disclose the production of positive ions in first half cycles and negative electrons in the other half cycles. Therefore, applicant's disclosure is not applicable to Koshimizu.

iv. The Examiner states on page 3 of the Office Action that the second source 130 of alternating voltage creates a bias on the electrode 110, this bias being a negative direct voltage. There is no indication in Koshimizu that the alternating

voltage from the source 130 creates a bias or that any such bias is a negative direct voltage.

v. The Examiner states on page 4 of the Office Action that "...it is anticipated by Koshimizu and common practice in he art that all wafers (or other articles) positioned on supports or electrodes would necessarily have a gap between the wafer/article and the support surface upon which the wafer/article is resting or electrically clamped." This is an unsupported statement by the Examiner. The Examiner should be required to provide support in the prior art for this statement, particularly since the Examiner states that this is "common practice in the art." If it is "common practice in the art," Examiner should have no difficulty in providing a prior art reference that discloses that it is "common practice." Furthermore, the sentence quoted above with the words "and where providing a direct current bias as a result of the first (134) and second (130) sources of alternating voltage" has no meaning, particularly since there is no verb.

vi. The Examiner then states on pages 4 and 5 of the Office Action:

> "This is demonstrated by Mountsier who shows a typical wafer-support interface (62/52; Figure 6). As such, when the structure recited in the reference is substantially identical to that of the claims, claimed properties or functions are presumed to be inherent."

Where does Mountsier "demonstrate" this? Applicant finds no demonstration to this effect in Mountsier. Certainly the structure 62/52 in Figure 6 of Mountsier does not disclose this.

vii. According to the Examiner on page 3 of the Office Action dated July 11, 2003, "the first (116) electrode is contiguous (neighboring) to, but spaced from, the wafer (W attached to the electrode 116 Figure 1, 3)." If the wafer is attached to the electrode 116, the wafer cannot be contiguous to the electrode. Furthermore, the wafer W is not "contiguous" or "neighboring" to the electrode 116. Koshimizu indicates in column 4, lines 8-10, that the electrode 116 "can fix a wafer W thereon." This prevents the wafer W and the electrode 116 from being contiguous. Furthermore, the drawings in Koshimizu show the wafer W as being disposed on the electrode 116.

viii. In column 4, lines 48-51, Koshimizu states:

> "Thus, predetermined high frequency powers are, preferably the same high frequency power is, applied to the first and second susceptors 110 and 116, respectively."

Koshimizu does not disclose that different amounts of power <u>are</u> applied to the susceptors 110 and 116. Even if different amounts of power should be applied to the susceptors 110 and 116, Koshimizu does not disclose which one of the susceptors receives the greater amount of power.

ix. According to the Examiner on page 6 of the Office Action dated July 11, 2003:

"Mountsier, as stated above, teaches a wafer support platform (52, Figure 5; column 4, lines 20 23) (sic) that provide a series relationship between two capacitors, one (68 dielectric gap; Figure 5; column 4, lines 20-23) having a high capacity impedance and the other (80/82 dielectric gap; Figure 6) having a low capacity impedance. In particular, because the wafer support 52 is made of an electrical insulator (ceramic, column 5, lines 8-20) capacitance across the stated points is established and the wafer (62) is electrically floated."

Applicant respectfully disagrees with the Examiner's position that Mountsier discloses two (2) capacitors and that, if there are two (2) capacitors, one has a high impedance and the other has a low impedance. This may be seen primarily from Figures 5, 6 and 7 in Mountsier. In Figure 5, the different elements shown have the following properties:

68 - gap filled with a gas such as helium or nitrogen

52 – ceramic disk

54 – layer of thermally conductive paste

56 – metal support disc

58 – layer of thermally conductive paste

60 – metallic coating disc

Figures 5 and 7 show a device for cooling the wafer 62. There is no discussion by Mountsier that the device provides electrical capacitors. Furthermore, the element 54 and 58 constitute thermally conductive paste. A thermal conductor is not necessarily an electrical conductor. If the elements 54 and 58 are electrically conductive, only the ceramic disc 52 is __dielectric. This prevents the device in Figures 5 and 7 from providing two (2) capacitors. If the elements 54 and 58 are electrical insulators, it is possible to have two (2) capacitors in series assuming that the metal support disc 56 serves as a conductive plate in each of the capacitors.

Even if Figure 5 and/or in Mountsier can be considered to provide two (2) capacitors, one does not have a high impedance and the other a low impedance. There is no statement in Mountsier to this effect. Furthermore, the dimensions of the elements in Figure 5 of Koshimizu do not support this. Figure 6 in Koshimizu is no help to the Examiner in this regard since Figure 6 shows only the wafer 62 and the ceramic disc 52.

Of course, it is possible that one of the thermally conductive plates 54 and 58 may be electrically conductive and the other may be electrically insulating. This further establishes that Mountsier has not provided a sufficient disclosure to support the Examiner's position since it provides different possibilities, not clarified, in either Koshimizu or Mountsier.

b. Differences between applicant's invention and Koshimizu (as applied specifically to the claims).

There are other significant reasons why claims 1-21 and 43-51 are allowable over Koshimizu. For example, claim 1 is allowable over Koshimizu because Koshimizu does not disclose a first electrode and magnetic members disposed relative to each other and to the molecules of an inert gas for ionizing molecules of the inert gas. There is also disclosure in Koshimizu that a second electrode and a wafer are disposed relative to each other and to the ions of the inert gas, and the second electrode is constructed, to obtain a movement of the ions to a surface of an insulating layer in the wafer at a low and controlled speed for an etching of the surface of the insulating layer by the ions at the low and controlled speed. Certainly neither the electrode 110 nor the electrode 116 in Koshimizu performs this function.

Claim 2 is dependent from claim 1 and is accordingly allowable over Koshimizu for the same reasons as claim 1. Claim 2 is also allowable over Koshimizu because Koshimizu does not disclose that a first electrical field and a magnetic field are disposed relative to each other and to the molecules of the inert gas for ionizing the molecules of the inert gas. Koshimizu also does not disclose that a second electrical field and the magnetic field are disposed relative to each other and to the ions of the inert gas to obtain the movement of the ions to the wafer at the low and controlled speed for an etching of the surface of the wafer by the ions at the low and controlled speed.

Claim 3 is allowable over Koshimizu because it is dependent from allowable claim 1. This is also true of claim 4.

Koshimizu does not disclose certain of the features recited in claim 7. For example, Koshimizu does not disclose first and second electrodes and a first source of an

alternating voltage for producing a direct negative voltage of a high magnitude on the first electrode for the creation of a first electrical field of a high magnitude in an enclosure. There is also disclosure in Koshimizu of a second source of an alternating voltage for producing a direct negative voltage of a low magnitude on the second electrode for the creation of a second electrical field of a low magnitude in the enclosure. No disclosure is further provided in Koshimizu that the wafer is disposed relative to the second electrode and to the ions of the inert gas in the enclosure to receive an etching of a low magnitude on the surface of an insulating layer in the wafer by the ions of the inert gas in the enclosure.

Because of its dependency from claim 7, claim 8 is allowable over Koshimizu for the same reasons as claim 7. Claim 8 is also allowable over Koshimizu because of the recitation of the operation of the first and second sources of alternating voltages respectively to produce a direct voltage of a high magnitude and a negative polarity on the first electrode and to produce a direct voltage of a low magnitude and a negative polarity on the second electrode and because of the recitation that the second electrode is disposed in a contiguous, but spaced, relationship to the wafer.

Applicant recites in claim 9 first and second electrical conductors and their respective dispositions relative to the first and second electrodes. Koshimizu does not disclose first and second electrical conductors and certainly does not disclose first and second electrical conductors with the characteristics recited in claim 9. Claim 9 is also allowable over Koshimizu because it is dependent from allowable claim 7.

Claim 11 is allowable over Koshimizu because Koshimizu does not disclose that the wafer is disposed in a spaced, but adjacent, relationship to the second electrode to create a first capacitor between the second electrode and the wafer and to create a second capacitor between the wafer and the ions of the inert gas in the enclosure. Claim 11 is also allowable over Koshimizu for the same reasons as discussed above with respect to claim 7 because it is dependent from claim 7.

Claim 14 is allowable over Koshimizu because Koshimizu does not provide the following elements such as recited in the claim: (a) a first source of an alternating voltage, (b) a first electrode, (c) a second source of an alternating voltage, (d) a second electrode and (e) the recitation in lines 16-19 that the second electrode and the wafer provide a first capacitor of a high impedance and that the wafer and the ions in the enclosure provide a second capacitor of a low impedance in a circuit to produce a current of a low magnitude for etching the surface of the insulating layer in the wafer.

Because of its dependency from allowable claim 14, claim 15 is allowable over Koshimizu for the same reasons as allowable claim 14. Claim 15 additionally recites that the first capacitor includes a dielectric of the molecules and ions of the inert gas and that the second capacitor includes a dielectric constituting the insulating layers in the wafer. Koshimizu does not disclose these features.

Claim 16 is allowable over Koshimizu because Koshimizu does not disclose first and second electrically conductive members such as recited in the claim. Claim 16 is also allowable over Koshimizu because of its dependency from allowable claim 14.

Claims 19 and 20 are dependent from allowable claim 14 and are accordingly allowable over Koshimizu for the same reasons as claim 14. Claim 20 is additionally allowable over Koshimizu for the same reasons as discussed above for claims 15 and 16.

In claim 21, the following recitations distinguish patentably over Koshimizu: (a) an enclosure including first and second electrodes, (b) a first voltage source for producing a voltage of a high magnitude on the first electrode to obtain a production of a high electrical field in the enclosure, (c) a second voltage source for producing a voltage of a low magnitude on the second electrode to obtain a production of a low electrical field in the enclosure and (d) a supply of molecules of an inert gas for introduction into the enclosure to cooperate with the first and second electrodes and magnetic members in obtaining an ionization of the gas molecules in the enclosure by the electrical and magnetic fields in the enclosure and in obtaining a movement of the ions in the enclosure to the insulating layer in the wafer at a speed to obtain a smooth and uniform etching of the surface of the insulating layer at a low rate without the creation of any pits in the surface of the insulating layer.

Claims 43-47 and 50 are directly or indirectly dependent from claim 21. Because of this, they are allowable over Koshimizu for the same reasons as claim 21. Claims 43-47 and 50 are also allowable over Koshimizu for these additional reasons:

Claim 43

The recitation of the first and second electrodes in cooperation with the magnetic field to produce the results specified in the claim.

Claim 44

The cooperation between the first voltage source and the first electrode to produce a strong negative direct voltage in the vicinity of the first electrode. The cooperation between the second voltage source and the second electrode to produce a weak negative direct voltage in the vicinity of the second electrode.

Claim 45

First and second electrical conducting members respectively in co-operative relationships with the first and second electrodes.

Claim 46

The relative disposition between first and second electrical conducting members and the first and second electrodes.

Claim 47

The relative disposition between the first electrical conducting member and the first electrode and between the second electrical conducting member and the second electrode.

Claim 50

The cooperative relationship between the first electrical conducting member and the first electrode and between the second electrical conducting member and the second electrode.

c. The effect of the combination of Mountsier with Koshimizu to reject applicant's claims as anticipated by Koshimizu.

The Examiner has referred to MPEP 2121.01 in indicating that Koshimizu is demonstrated by Mountsier. MPEP 2121.01 indicates that a second prior art reference may be combined with a first prior art reference when the first prior art reference does not provide an enabling disclosure. Apparently the Examiner believes that Koshimizu's patent, by itself, does not provide an enabling disclosure. This is certainly not a factor in favor of the citation of Koshimizu against applicant's claims. The Examiner is then applying Mountsier to make the Koshimizu disclosure enabling. This is apparently what the Examiner means by the words "demonstrated by Mountsier" in the first sentence of Section 3 on page 2 of the Office Action dated July 11, 2003.

One problem with respect to the Examiner's position is that the Examiner does not specify in the Office Action dated July 11, 2003 what is not enabling in Koshimizu with respect to applicant's claims 1-4, 7-9, 11, 14-16, 19-21, 43, 44, 45, 46, 47 and 50 and what Mountsier contributes to make Koshimizu enabling with respect to the discussion by the Examiner in Section 3 on pages 2-5 of the Office Action dated July 11, 2003. The only mention of Mountsier by the Examiner on pages 2-5 of the Office Action appears to be on page 3, line 6, and the next-to-last line on page 4 of the Office Action. These references to Mountsier are so vague that they have no meaning. Furthermore, the disc 52 and the wafer 62 in Figures 5-7 of Mountsier do not define first and second capacitors such as recited by applicant in the claims.

At any rate, claims 1-4, 7-9, 11, 14-16, 19-21, 43-47 and 5D are allowable over Mountsier for all of the reasons specified above as to why these claims are allowable over

Koshimizu. Since Mountsier is lacking the same features in applicant's claims as Koshimizu, Mountsier cannot "demonstrate" what Koshimizu does not teach.

Claims 5, 6, 10, 12, 13, 17, 18, 20, 48, 49 and 51 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Koshimizu in view of Mountsier. All of claims 5, 6, 10, 12, 13, 17, 18, 20, 48, 49 and 51 are dependent from claims allowable over Koshimizu as specified above and are accordingly allowable over the combination of Koshimizu and Mountsier for the same reasons as specified above for the claims from which they are dependent.

Claims 5, 6, 13, 20 and 51 also include a recitation of first and second electrical conducting members. Neither Koshimizu nor Mountsier discloses these electrical conducting members. This is another reason why claims 5, 6, 13, 20 and 51 are allowable over the combination of Koshimizu and Mountsier.

Claims 48 and 49 recite a series relationship between two (2) capacitors, one having a high capacity impedance and the other having a low capacity impedance wherein the high capacity impedance limits the energy providing for the etching of the surface of the insulating layer in the wafer. Neither Koshimizu nor Mountsier discloses two (2) capacitors having characteristics such as recited in claims 48 and 49. Contrary to the position of the Examiner, Mountsier does not teach two (2) capacitors in a series relationship, one capacitor having a high capacitor impedance and the other capacitor having a low capacitor impedance. The structure shown in Figures 5 and 6 of Mountsier does not provide two (2) capacitors in series, one with a high capacity impedance and the other with a low capacity impedance. Furthermore, the structure shown in Figures 5 and

6 of Mountsier is for cooling and not for providing electrical capacitance. For example, Mountsier does not disclose whether layers 54 and 52 of thermally conductive paste are made from an electrically dielectric material or an electrically conductive material.

Furthermore, the recitation that the high capacity impedance limits the energy providing for the etching of the surface of the insulating layer in the wafer constitutes a structural limitation, not a functional limitation. Neither Koshimizu nor Mountsier discloses this structural limitation.

Koshimizu states the following in column 4, lines 48 and 49:

> ". . . Thus, predetermined high frequency powers are, preferably the same high frequency power is, applied to the first and second susceptors 110 and 116, respectively."

Applicant agrees with the Examiner that Koshimizu infers by the word "preferably" that one of the electrodes 110 and 116 can receive a different amount of power than the other electrode. But there is no indication of which one of the electrodes can receive the greater amount of power.

Applicant is not certain what the Examiner means by the word "demonstrated" on page 3, line 6 of the Office Action dated July 11, 2003. Apparently, the Examiner is not satisfied with Koshimizu as a single reference. Since the Examiner has had to cite Mountsier in combination with Koshimizu, the claims should not be considered as anticipated by Koshimizu. Rather, the claims should be considered patentable over the combination of Koshimizu and Mountsier since Koshimizu does not disclose a number of

the features recited by applicant in the claims and Mountsier does not disclose the same features that Koshimizu fails to disclose.

d. The effect of the combination of Mountsier and applicant's alleged admission on page 12, lines 1-9 of applicant's specification to reject the claims.

Applicant has indicated above in detail all of the failures of Mountsier to disclose specific features recited in applicant's claims. As will be seen, these failures are many. These same features apply equally as well to applicant's alleged admissions on page 12, lines 1-9 of applicant's specification. The differences between applicant's invention as disclosed and claimed in this application and applicant's alleged admission on page 12, lines 1-9 of applicant's specification constitute the differences between success and failure. Applicant's prior embodiment did not provide a smooth and even etching of a surface of an insulating layer in a wafer. Applicant's apparatus as disclosed and claimed in this applicant provides a smooth and even etching of a surface of an insulating layer in a wafer.

e. The law relating to the combination of Koshimizu and Mountsier, and the combination of Mountsier and applicant's alleged admission, to reject the claims.

In order for different prior art references to be combined to reject a claim, the references have to disclose or suggest the combination recited in the claim. ACS Hospitality Systems, Inc. v. Montefiore Hospital, 732 F.2d 1572, 221 USPQ 929 (Fed. Cir. 1984). As the Federal Circuit indicated in the ACS case at 732 F.2d 1577, 1579, 221 USPQ 929, 933:

> "Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent some teaching or suggestion supporting the combination. Under Section 103, teaching of references can be combined only if there is some suggestion or incentive to do so."

See also In re Fine, 837 F.2d 1071, 5 USPQ 2d 1596, (Fed. Cir. 1988) and In re Jones, 1958 F.2d 347, 21 USPQ 2d 1941 (Fed. Cir. 1992) in support of the holding in the ACS case. Neither Koshimizu nor Mountsier cited by the Examiner to reject the claims in this application discloses or suggests certain of the features recited in the claims. Furthermore, neither Mountsier nor applicant's alleged admissions discloses or suggests certain of the features recited in the claims. The references cannot accordingly be combined to reject the claims.

f. Reconsideration and allowance of the application are respectfully requested.

Respectfully submitted,

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